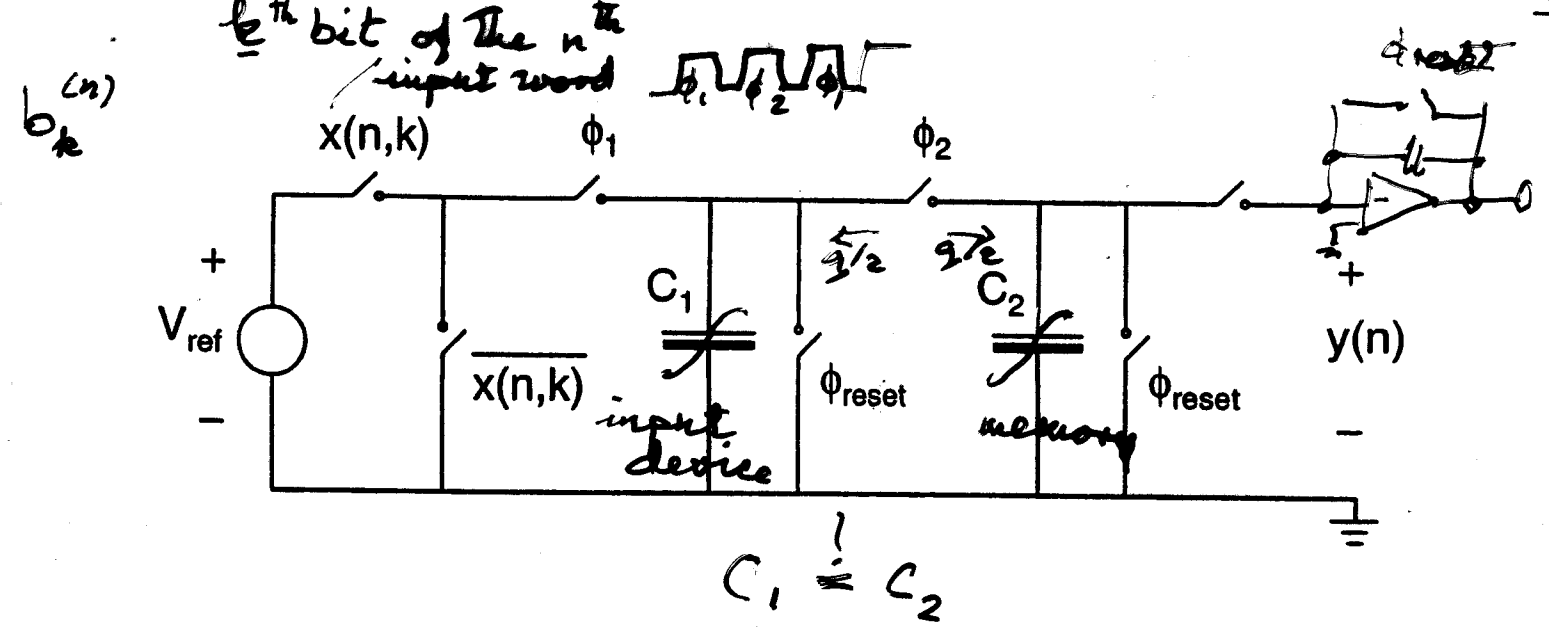
T N.1 throughput = 1/T latency

Parallel, serial, pipelined operation

ERROR CANCELLATION I

ANALOG ERROR CAN SOMETIMES BE CANCELLED EVEN IF IT IS UNKNOWN. CDS IS AN EXAMPLE. FOR SOME SIMPLE CIRCUITS, MISMATCH ERROR CAN ALSO BE CANCELLED. EXAMPLE 1: SERIAL SC DAC

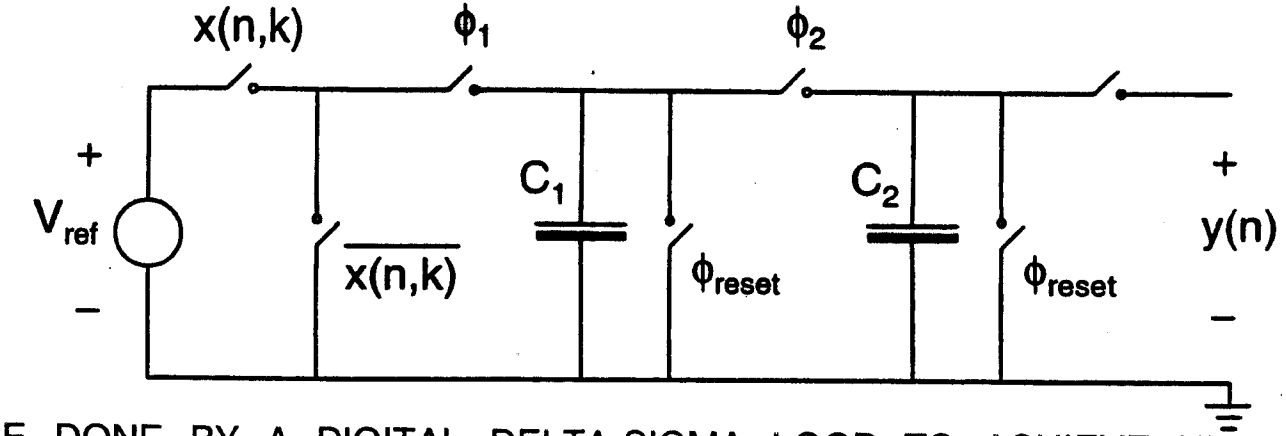


LSB ENTERS FIRST, MSB LAST. SIMPLE, ROBUST, NO GLITCH. HOWEVER, C MISMATCH CAUSES HARMONIC DISTORTION. THE ERROR OF THE ANALOG OUTPUT IS PROPORTIONAL TO THE RELATIVE MISMATCH D = (C1 - C2)/(C1 + C2). (TO A FIRST-ORDER APPROXIMATION, FOR |D| << 1.) HENCE, PERFORMING THE CONVERSION TWICE, WITH OPPOSITE ROLES FOR C1 & C2, AND ADDING THE ANALOG OUTPUTS, WILL CANCEL THE FIRST-ORDER ERROR.

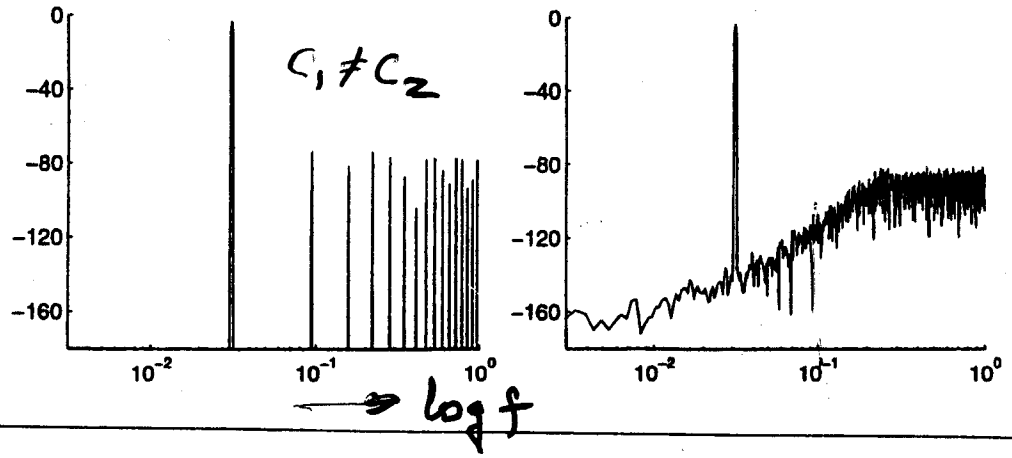
$$Q_{out} = C_1 V_{ref} \sum_{i=1}^{N} b_i 2^{-i}$$

SPECTRAL ERROR SHAPING III

EXAMPLE 2: THE ERROR SIGNAL OF THE 2-CAPACITOR DAC SHOWN EARLIER CAN BE FILTERED, **SINCE** THERE IS AN OPTION IN EACH BIT CONVERSION TO INTERCHANGE THE CS:



THIS CAN BE DONE BY A DIGITAL DELTA-SIGMA LOOP TO ACHIEVE HIGH-ORDER ERROR SPECTRUM SHAPING. THE OUTPUT SPECTRA BEFORE AND AFTER SHAPING:



A Quasi-Passive CMOS Pipeline D/A Converter

FONG-JIM WANG, MEMBER, IEEE, GABOR C. TEMES, FELLOW, IEEE AND SIMON LAW, MEMBER, IEEE

Abstract — A novel pipeline digital-to-analog converter (DAC) configuration, based on switched-capacitor techniques, is described. An n-bit D/A conversion can be implemented by cascading $n+1$ unit cells. The device count of the circuit increases linearly, not exponentially, with the conversion accuracy. The new configuration can be pipelined. Hence, the conversion rate can be increased without requiring higher clock rate. An experimental 10-bit DAC prototype has been fabricated using a 3-μm CMOS process. The results show that high-speed, high-accuracy, and low-power operation can be achieved without special process or postprocess trimming.

N + 1 Cs

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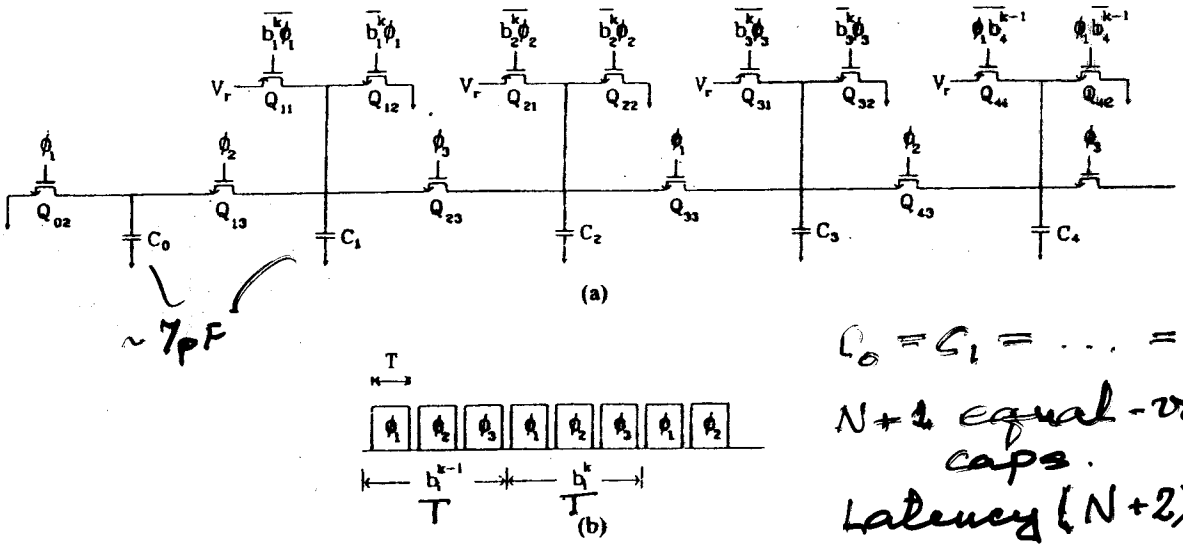
LSB



$C_0 = C_1 = \ldots = C_{N+1}$

N+1 equal-valued caps.

Latency (N+2)T.

Fig. 1. (a) Proposed quasi-passive pipeline D/A converter. (b) Clock timing of the proposed converter.

No glitch.

Very fast!

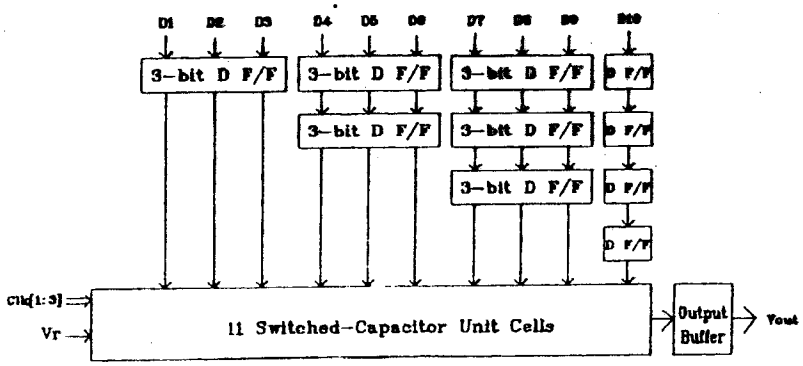


Fig. 2. System block diagram of 10-bit D/A converter.

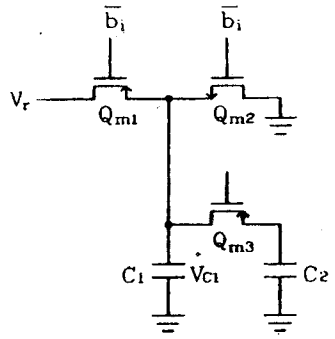


Fig. 3. The mth stage of the converter.

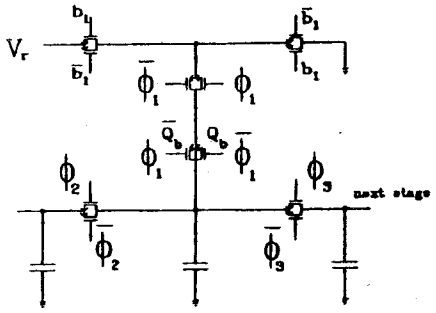


Fig. 4. Unit cell of a CMOS implementation.

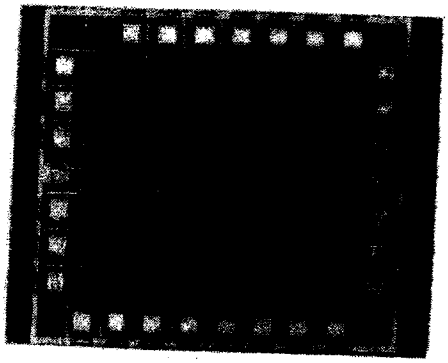


Fig. 5. Photomicrograph of the prototype chip.

Fig. 6. Output waveform for a ramp input signal.

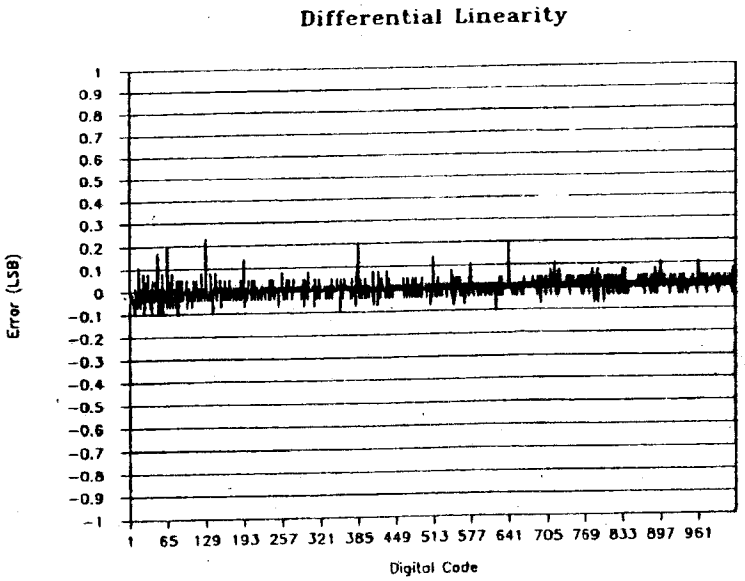


Fig. 7. Differential nonlinearity response.

ERROR SOURCES

I. CAPACITOR MISMATCHING

SOLUTION:

LARGE UNIT CAPACITORS

CAREFUL LAYOUT

II. NONZERO SWITCH ON–RESISTANCE

SOLUTION:

LARGE TRANSISTOR SIZE

III. CLOCK FEEDTHROUGH CHARGES

NO EFFECT ON LINEARITY (gain & offset errors only).

Dummy switches reduce charge injection:

IV. Capacitive coupling btw. C_i & C_{i+1} : guard strips help.

V. Last switch must be "on" when output is sampled, to avoid charge injection from last switch.

VI. Buffer must be N+1-bit linear.